# 328612(28)

# B. E. (Sixth Semester) Examination, 2020

(Old Scheme)

(Branch: Et & T)

# ADVANCED ELECTRONIC CIRCUITS

Time Allowed: Three hours

Maximum Marks: 80

Minimum Pass Marks: 28

Note: Attempt all questions. Part (a) is compulsory from each questions. Attempt any two parts from (b), (c) and (d).

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# Unit - I

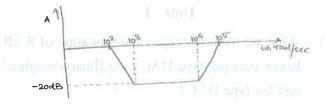
1. (a) What are the advantages and limitation of R-2R ladder network type DAC over Binary-weighted resistor type DAC?

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- (b) Explain the operation of 3-bit R-2R type DAC and derive the expression for the output voltage.
- (c) Explain Dual-slope type ADC with the help of block diagram.
- (d) Explain the operation of successive approximation type ADC with the help of block diagram.

#### Unit - II

- 2. (a) Define bilinear transfer function.
  - (b) Design a circuit to provide a set of three phase 60 Hz voltage each separated by  $120^{\circ}$  and equal in magnitude. Assume  $C = 1 \,\mu\text{f}$ .
  - (c) Explain Biquad circuit with circuit diagram and also derive an expression for frequency response. 7
  - (d) For the Bode plot given below, find the transfer function and design the corresponding filter. Use all capacitors of value of 0.01 μf.



# [3]

#### Unit - III

- **3.** (a) What is RC-CR transformation.
  - (b) Describe the sallen and key circuit with three design strategies.
  - (c) Defie sensitivity. Explain the sensitivity analysis of sallen and key circuit.
  - (d) If  $\alpha_{\text{max}} = 0.25 \text{ dB}$ ,  $\alpha_{\text{min}} = 18 \text{ dB}$ ,  $f_p = 1000 \text{ Hz}$ ,  $f_s = 1400 \text{ Hz}$  for Butterworth LPF. Determine order of filter, Half power frequency, attenuation at passband and attenuation at the edge of stopband.

# Unit - IV

- 4. (a) Define Lock Range and capture Range.
  - (b) Discuss the various application of PLL.
  - (c) With the help of functional diagram explain the operation of PLL 565.
  - (d) A PLL has a VCO with  $K_0 = 25$  KHz/v and  $F_c = 50$  KHz. The amplifier gain is A = 2 and the phase detector has a maximum output voltage swing

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# [4]

	of $+0.7$ volt. Find the Lock range of PLL. Assume filter gain equal to unity.	7
	Unit - V	
5.	(a) Define multiplier.	2
	(b) Discuss the various application of analog multiplier.	7
	(c) Explain the basic method of performing analog multiplication.	7
	(d) Explain the various characteristics of multiplier	7
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	(d) A PLL law a VCO with $K_0=25$ k Hz/v and F = $-1$ kHz/v and fix the property of the place defector being assimpt subpit soluble assimpt	